SPECIFICATION AMENDMENTS:

Please amend the paragraph beginning on page 29, line 16 as follows:

Referring now to FIG. 9, an antenna system 150 of the invention is shown for a phased array 152 of n elements 152_1 to 152_n employing double variable delay, n being an arbitrary positive integer. A first splitter 154_1 receives an input signal Vin, and splits it into two signals one of which has twice the power of the other. Of these two signals, the higher powered signal is routed to a first variable phase shifter 156_1 and the lower powered signal to a first fixed phase shifter 158_1 The first fixed phase shifter 158_1 provides an output signal via a second fixed phase shifter 158_2 to a second splitter 154_2, which splits it into n signal fractions a1 to an for output via a bus indicated by Path P. The first variable phase shifter 156_1 provides an output signal to a third splitter 154_3 which splits it into n signal fractions b1 to bn. Signal fractions b2 to bn are output via a third ~~first~~ fixed phase shifter 158_3 and a bus indicated by Path Q. Signal fraction b1 has equal power to that of the signal fed to the first fixed phase shifter 158_1, and it is routed to a second variable phase shifter 156_2 and thence to a fourth splitter 154_4, which splits it into n signal fractions c1 to cn for output via a bus indicated by Path R. The buses indicated by Paths P, Q and R have Na, Nb and Nc individual conductors respectively.